Product Introduction

LS98003 is a general and configurable digital logic chip, characterized by small size, ultra-low power consumption, and high reliability. Customers can design chips according to their functional requirements, configure the connections between the simulation and logic functional modules inside LS98003, and burn the design into the internal NVM (Non-Volatile Memory). The internal functional blocks are as follows:

- Seven Combination Function Macrocells
  - Two 2-bit LUT/DFF
  - One 2-bit LUT/Pattern Generator
  - Two 2-bit LUT/Edge Detector
  - One 4-bit LUT/DFF
  - One 3-bit LUT/Pipe Delay
- Eight Multi-Function Blocks
  - Seven Selectable 3-bit LUT/DFF + 8-bit Counter/Delay
  - One Selectable 4-bit LUT/DFF + 16-bit Counter/Delay
- I^2C Protocol Interface
- Two Internal Oscillators
  - One 2MHz Oscillator
  - One 20KHz Oscillator
- Power-On Reset
- The Read Protection Function
- Wide Range Power Supply: 1.71V to 5.5V
- Operating Temperature Range: -40℃ to 85℃
- RoHS Compliant/Halogen-Free
- Package: TQFN-8L: 1.3mm x 1.3mm x 0.55mm, 0.4mm pitch
  DFN-8L: 2.0mm x 2.0mm x 0.75mm, 0.5mm pitch

Applications

- Consumer electronics
- Data Communications Equipment
- TWS headphone or One Wire communication assistance
- Carrier single line communication
- IO Expanders

Glossary

C

- CLK: Clock
- CNT: Counter

D

- DFF: D Flip-Flop
- DLY: Delay

E

- ESD: Electrostatic discharge

F

- FSM: Finite State Machine

G

- GPI: General Purpose Input
- GPIO: General Purpose Input/Output
- GPO: General Purpose Output

I

- IN: Input
- IO: Input/Output

L

- LSB: Least Significant Bit
- LUT: Look-Up Table
- LV: Low Voltage

M

- MSB: Most Significant Bit
- MUX: Multiplexer
- MFB: Multi-Function Block
- MSL: Moisture Sensitivity Level

N

- nRST: Reset
- NVM: Non-Volatile Memory

O

- OE: Output Enable
- OSC: Oscillator
- OUT: Output

P

- PDWM: Power-down
- PGen: Pattern Generator
- POR: Power-On Reset
- PP: Push-Pull
- PDLY: Programmable Delay

S

- SCL: I^2C Clock Input
- SDA: I^2C Data Input/Output
- SLA: Slave Address
- SMT: With Schmitt Trigger

V

- VREF: Voltage Reference

W

- WOSMT: Without Schmitt Trigger

Contents

1. System Block

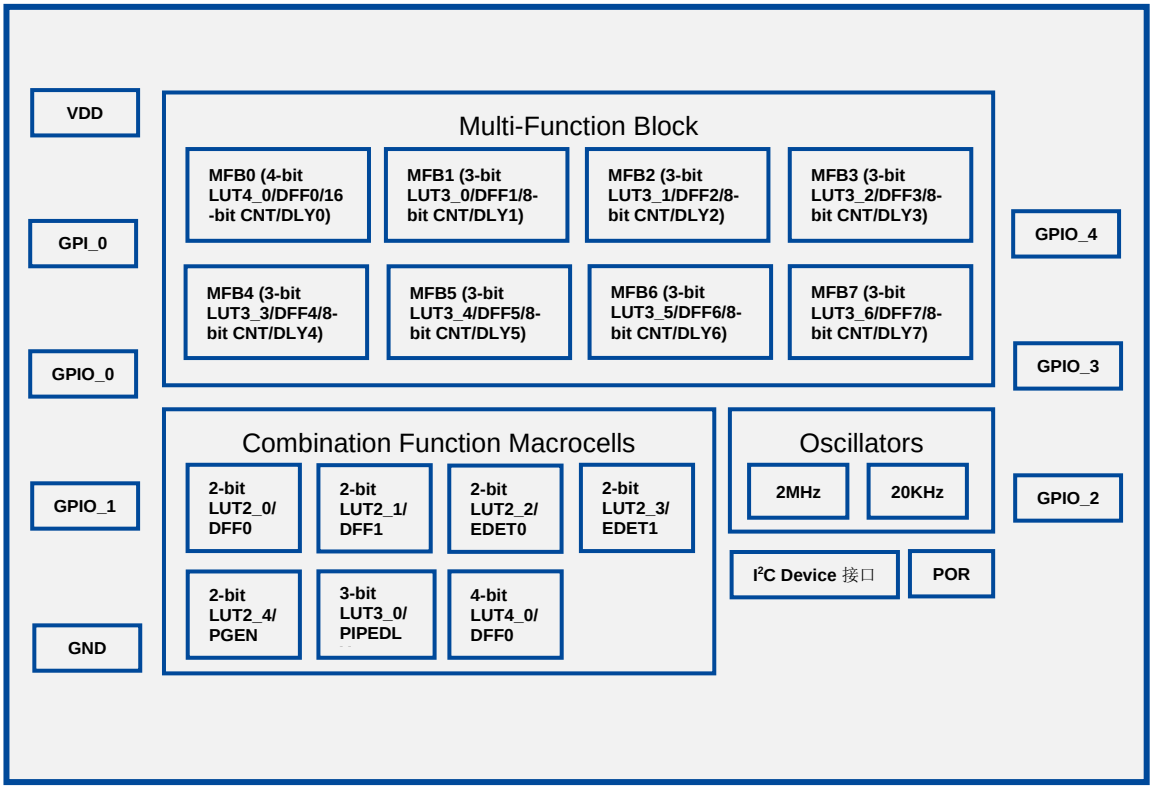


Figure 1：Block Diagram

2. Pin Definition

2.1 Pin Configuration-TQFN-8L

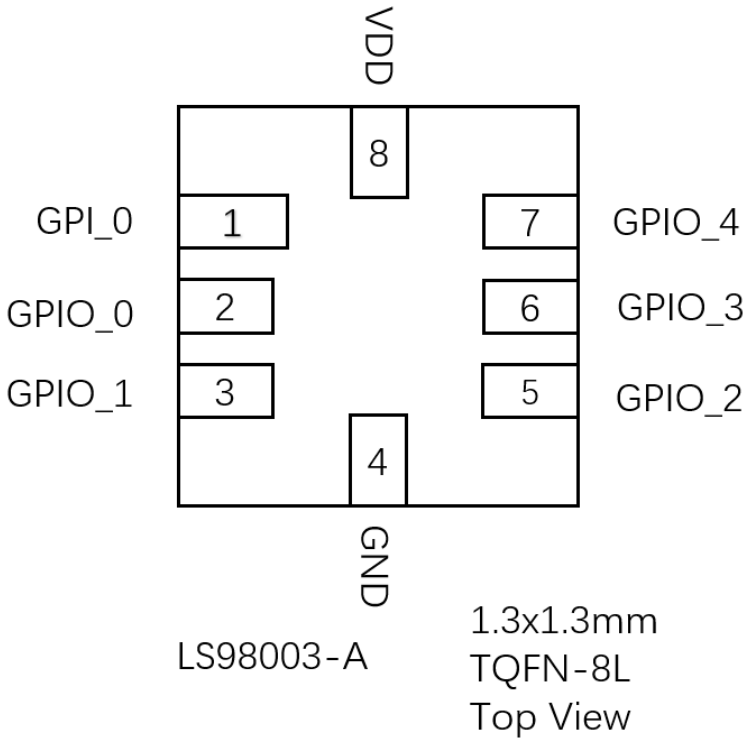


Figure 2：TQFN-8L (Top View)

Table 1：LS98003-A PIN Description

PIN#(A)	Name	Function
8	VDD	Power
1	GPI_0	GPI,VPP(program Power)
2	GPIO_0	GPIO,I^2C SCL. Supports up to 5.5V (can be higher than VCC)
3	GPIO_1	GPIO,I^2C SDA.
4	GND	Power GND
5	GPIO_2	GPIO with OE,Support OD,Push Pull
6	GPIO_3	GPIO with OE, Support OD,Push Pull
7	GPIO_4	GPIO with OE, Support OD,Push Pull

2.2 Pin Configuration-DFN-8L

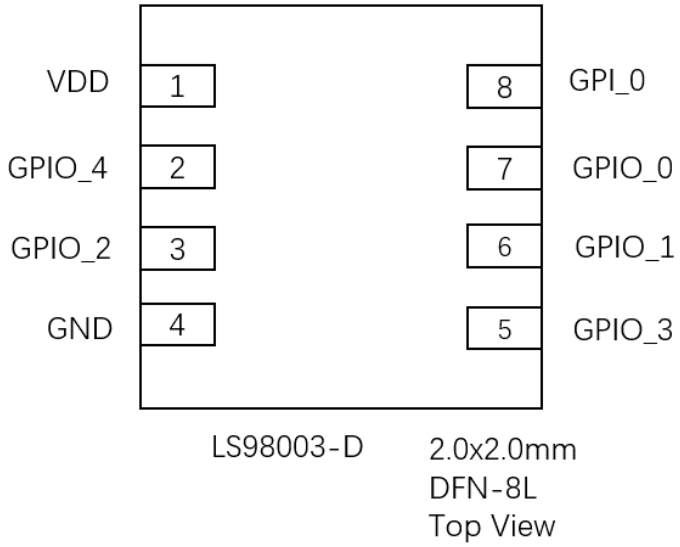


Figure 3: DFN-8L (Top View)

Table 2: LS98003-D PIN Description

PIN#(D)	Name	Function
1	VDD	Power
2	GPIO_4	GPIO with OE
3	GPIO_2	GPIO with OE
4	GND	Ground
5	GPIO_3	GPIO with OE
6	GPIO_1	GPIO,I^2C SDA
7	GPIO_0	GPIO,I^2C SCL
8	GPI_0	GPI,VPP(program Power)

3. Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Analog and digital grounds must be connected together on the PCB board. The place of connection depends on customers' schematic. For application cases with low digital current of LS98003, both AGND and GND should be connected to analog ground plane.

Table 3: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VDD to GND	-0.3	7	V
IO maximum voltage	-0.3	7	V
VDD to GND Maximum DC current	--	90	mA
Input leakage current	--	1000	nA
Storage temperature	-65	150	℃
Junction temperature	--	150	℃
Moisture Sensitivity Level (MSL)	1		--

3.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Min	Max	Unit
VDD Supply Voltage	1.71	5.5	V
Operating Temperature	-40	85	℃
Maximum voltage input to Pin	-0.2	VDD+0.3 5.5V PIN3	V
Capacitor Value at VDD	0.1	--	uF

3.3 Electrostatic Discharge Ratings

Table 5: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Charged Device Model)	500	--	V
ESD Protection (Human Body Model)	2000	--	V

3.4 Electrical Characteristics

表 6：Electrical Characteristics (VDD: 1.8V±5%, Temp: -40~85°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.3	1.43	1.6	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.55	1.03	1.35	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	0.8	--	ms
I_{stand_by}		T=+25 °C	--	50	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	0.83	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.46	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.42	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100 µA, 1X Drive	1.69	--	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive	1.70	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100 µA, 1X Drive	--	--	0.012	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive	--	--	0.006	V
		Open Drain, I_{OL} = 100 µA, 1X Drive	--	--	0.004	V
		Open Drain, I_{OL} = 100 µA, 2X Drive	--	--	0.002	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = VDD - 0.2, 1X Drive	0.81	--		mA
		Push-Pull, V_{OH} = VDD - 0.2, 2X Drive	1.6	--		mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.15 V, 1X Drive	1.1	--		mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive	2.1	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive	3.2	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive	6.3	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	2MHz OSC	T=+25 °C	--	1.5	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	2	--	MHz
		T=-40 °C to +85 °C	1.88	--	2.12	MHz
Power Consumption		T=+25 °C	--	23	--	uA
		T=-40 °C to +85 °C	--	--	30	uA
Power-On time	20KHz OSC	T=+25 °C	--	60	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	20.5	--	KHz
		T=-40 °C to +85 °C	19.27	--	21.73	KHz
Power Consumption		T=+25 °C	--	2.4	--	uA
		T=-40 °C to +85 °C	--	--	3.4	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

表 7：Electrical Characteristics (VDD: 3.3V±10%, Temp: -40~85°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.67	1.80	1.92	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.95	1.25	1.54	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.20	--	ms
I_{stand_by}		T=+25 °C	--	97	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	0.92	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.77	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.45	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 3 mA, 1X Drive	2.60	--	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive	2.80	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 3 mA, 1X Drive	--	--	0.25	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive	--	--	0.22	V
		Open Drain, I_{OL} =3 mA, 1X Drive	--	--	0.12	V
		Open Drain, I_{OL} =3 mA, 2X Drive	--	--	0.089	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = 2.4 V, 1X Drive	5	--	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	10	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	5	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	10	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	15	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	30	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	2MHz OSC	T=+25 °C	--	1.5	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	2	--	MHz
		T=-40 °C to +85 °C	1.88	--	2.12	MHz
Power Consumption		T=+25 °C	--	31	--	uA
		T=-40 °C to +85 °C	--	--	40	uA
Power-On time	20KHz OSC	T=+25 °C	--	52	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	20	--	KHz
		T=-40 °C to +85 °C	18.8	--	21.2	KHz
Power Consumption		T=+25 °C	--	2.7	--	uA
		T=-40 °C to +85 °C	--	--	3.4	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

表 8：Electrical Characteristics (VDD: 5V±10%, Temp: -40~85°C)

Parameter		Condition/Note	Min.	Typ.	Max.	Unit.
POR						
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	1.67	1.80	1.92	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.95	1.25	1.54	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.20	--	ms
I_{stand_by}		T=+25 °C	--	155	--	nA
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7*VDD	--	--	V
		Logic Input with Schmitt Trigger	0.8*VDD	--	--	V
		Low-Level Logic Input	1.00	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.3*VDD	V
		Logic Input with Schmitt Trigger	--	--	0.2*VDD	V
		Low-Level Logic Input	--	--	0.86	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	--	0.54	--	V
I_{LKG}	Input leakage (Absolute Value)	--	--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 5 mA, 1X Drive	4.04	--	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive	4.20	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 5 mA, 1X Drive	--	--	0.29	V
		Push-Pull, I_{OL} = 5 mA, 2X Drive	--	--	0.21	V
		Open Drain, I_{OL} = 5 mA, 1X Drive	--	--	0.15	V
		Open Drain, I_{OL} = 5 mA, 2X Drive	--	--	0.114	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push-Pull, V_{OH} = 2.4 V, 1X Drive	19	--	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	38	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	7	--	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	14	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	21	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	42	--	--	mA
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	KΩ
		10 k Pull Up	--	10	--	KΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	KΩ
		10 k Pull Down	--	10	--	KΩ
Oscillators						
Power-On time	2MHz OSC	T=+25 °C	--	1.5	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	1.97	--	MHz
		T=-40 °C to +85 °C	1.85	--	2.09	MHz
Power Consumption		T=+25 °C	--	45	--	uA
		T=-40 °C to +85 °C	--	--	57	uA
Power-On time	20KHz OSC	T=+25 °C	--	50	--	uS
$Freq_{Accuracy}$		T=+25 °C	--	20	--	KHz
		T=-40 °C to +85 °C	18.8	--	21.2	KHz
Power Consumption		T=+25 °C	--	3.6	--	uA
		T=-40 °C to +85 °C	--	--	4.6	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

表 9：I²C 引脚时序参数, (VDD: 1.8V±5%, Temp: -40℃ ~ 85℃)

Parameter	Description	Condition	Standard-Mode		Unit
			Min	Max	
F_{SCL}	Clock Frequency, SCL		--	100	KHz
t_{LOW}	Clock Pulse Width Low		4.7	--	us
t_{HIGH}	Clock Pulse Width High		4.0	--	us
t_I	Input Filter Spike Suppression (SCL,SDA)		--	70	ns
t_{AA}	Clock Low to Data Out Valid		--	3.45	us
t_{BUF}	Bus Free Time between Stop and Start		4.7	--	us
t_{HD_STA}	Start Hold Time		4.7	--	us
t_{SU_STA}	Start Set-up Time		4.7	--	us
t_{HD_DAT}	Data Hold Time		0	--	ns
t_{SU_DAT}	Data Set-up Time		250	--	ns
t_R	Inputs Fail Time		--	1000	ns
t_F	Inputs Rise Time		--	300	ns
t_{SU_STO}	Stop Set-up Time		4.0	--	us
t_{DH}	Data out Hold Time		50	--	ns
Note: Timing Diagram can be found in the Figure 20.					

表 10：I²C 引脚时序参数, (VDD:2.3V ~ 5.5V, Temp: -40℃ ~ 85℃)

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	KHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL,SDA)	VDD=2.5V±8%	--	95	--	168	ns
		VDD=3.3V±10%	--	95	--	157	ns
		VDD=5V±10%	--	111	--	156	ns
t_{AA}	Clock Low to Data Out Valid		--	900	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Fail Time		--	300	--	120	ns
t_F	Inputs Rise Time		--	300	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	260	--	ns
t_{DH}	Data out Hold Time		50	--	50	--	ns
Note: Timing Diagram can be found in the Figure 20.							

4. IO Pins

The LS98003 has a total of 5 GPIO Pins which can function as either a user-defined Input or Output, as well as serve as a special function (such as outputting the voltage reference) and 1 GPI Pin.

4.1 GPI Pin

GPI_0 serve as General Purpose Input Pin, it's internal block diagram is shown in Figure 4.

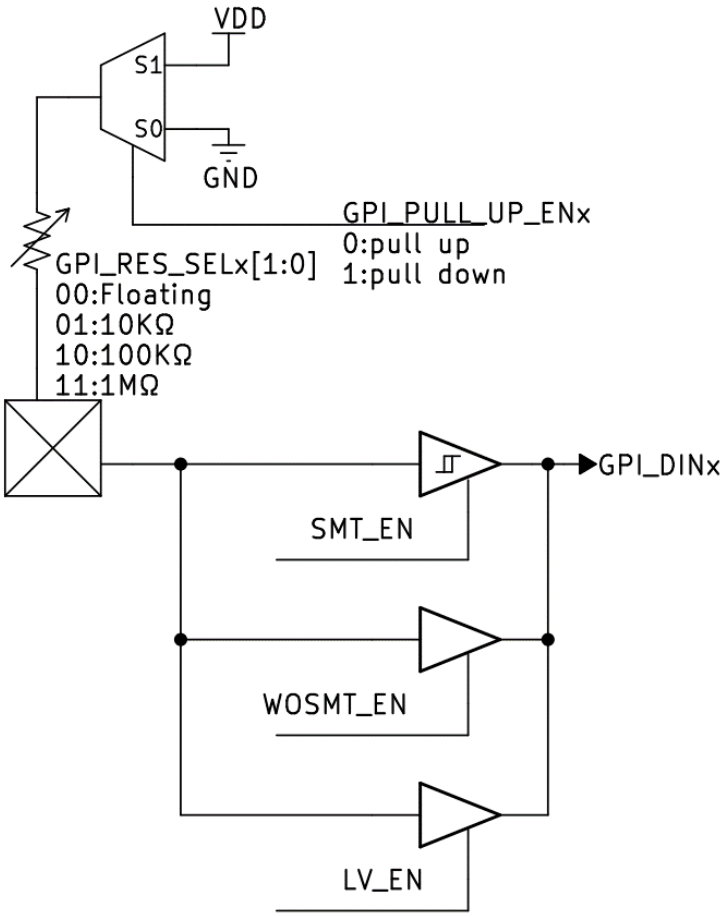


Figure 4: GPI_0 Structure Diagram

4.2 GPIO Pins

GPIO_0, GPIO_1, GPIO_2, GPIO_3, and GPIO_4 serve as General Purpose IO Pins.

For the GPIO_0、GPIO_1, which has I²C features on it, the system block diagram is shown in Figure 5.

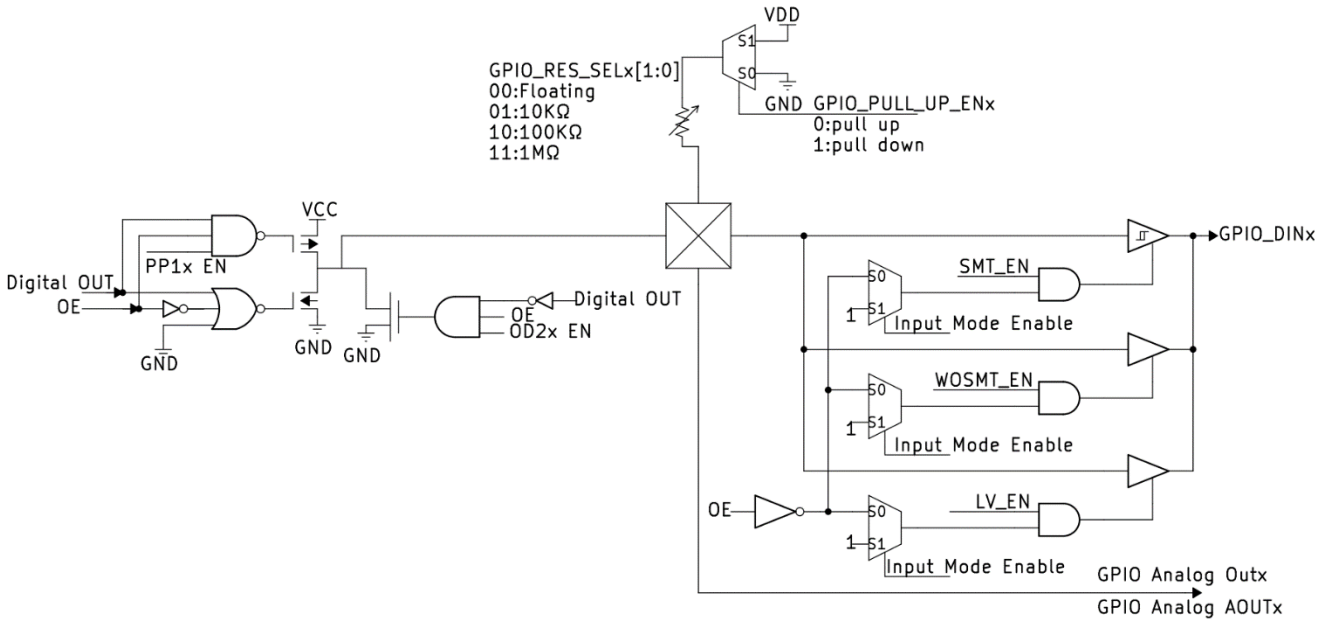


Figure 5：IO with I²C Mode IO Structure Diagram

For the GPIO_2, GPIO_3, and GPIO_4, the system block diagram is shown in Figure 6.

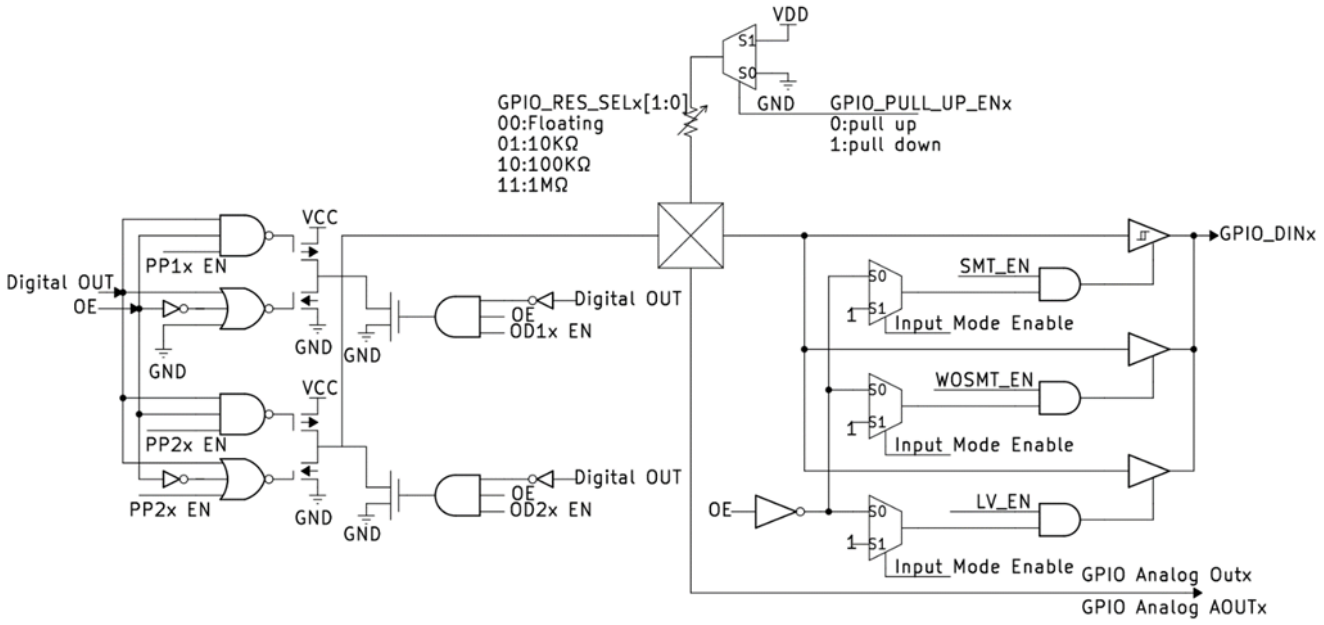


Figure 6：GPIO with OE Structure Diagram

5. Connection Matrix

LS98003 has an interconnection matrix internally, which can be used for internal resource connections and matrix connections through register configuration. These registers can be burned through OTP.

The input of the connection matrix comes from internal resources or the output of the connection matrix, while the output of the connection matrix is the input of internal resources or the connection matrix. The output of each connection matrix is configured through a set of registers.

6. Combination Function Macrocells

The LS98003 has seven combination function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Two 2-bit LUT/DFF
- One 2-bit LUT/Pattern Generator
- Two 2-bit LUT/Edge Detector
- One 3-bit LUT/Pipe Delay
- One 4-bit LUT/DFF with nRST/nSET

6.1 2-bit LUT/DFF

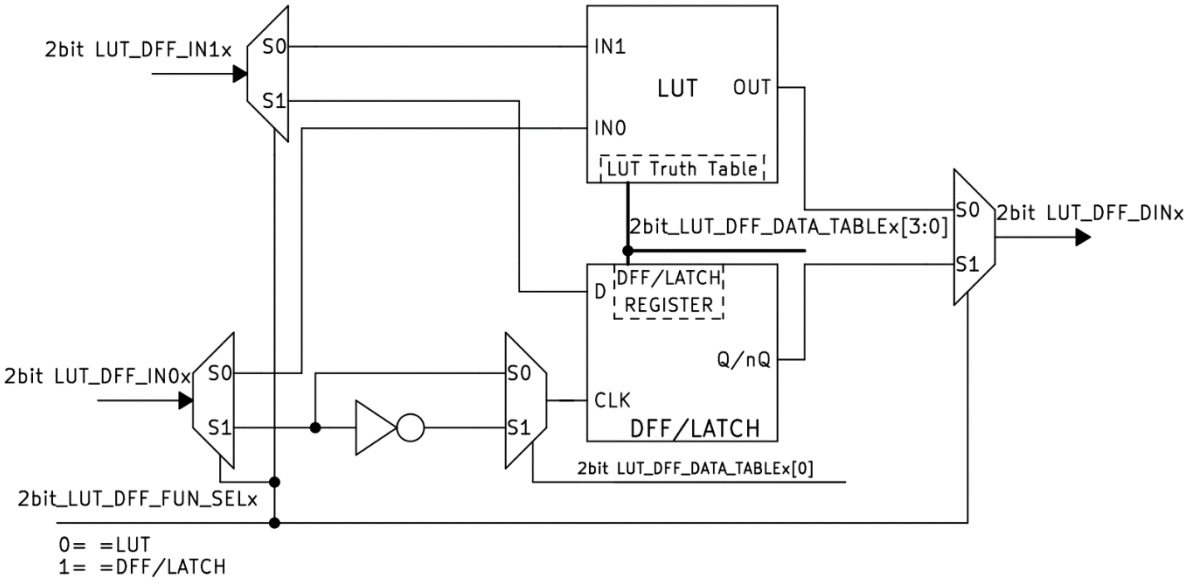


Figure 7：2-bit LUT/DFF

6.2 2-bit LUT/Pattern Generator

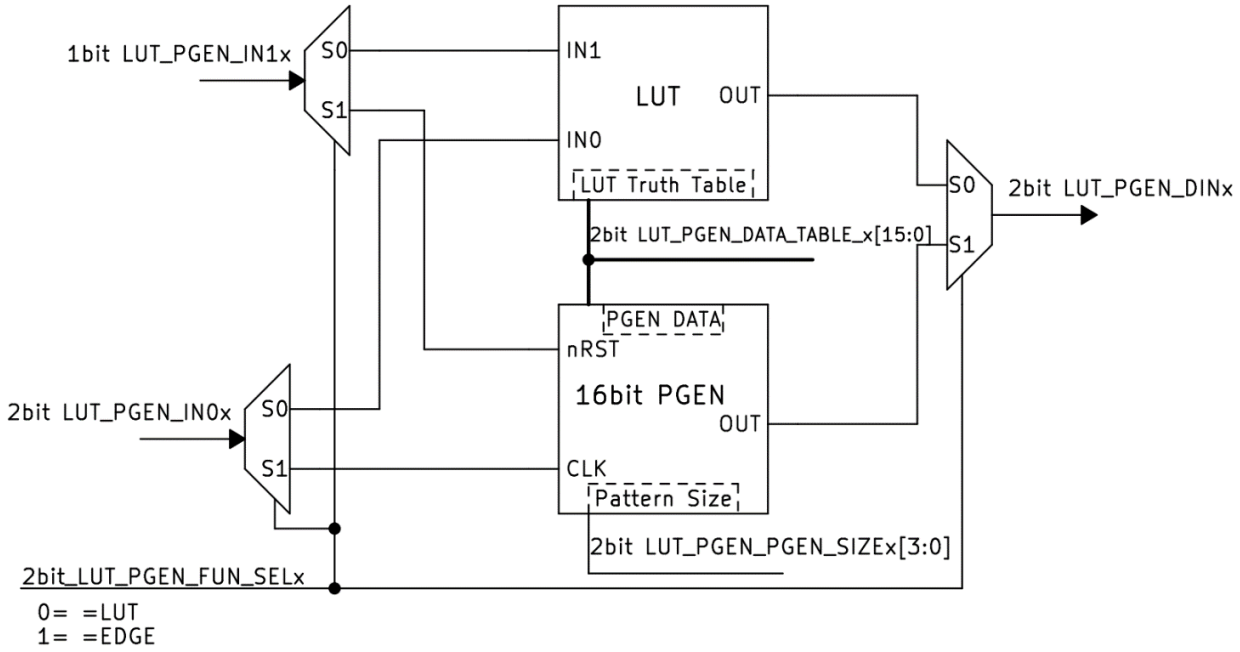


Figure 8：2-bit LUT/Pattern Generator

6.3 2-bit LUT/Edge Detector

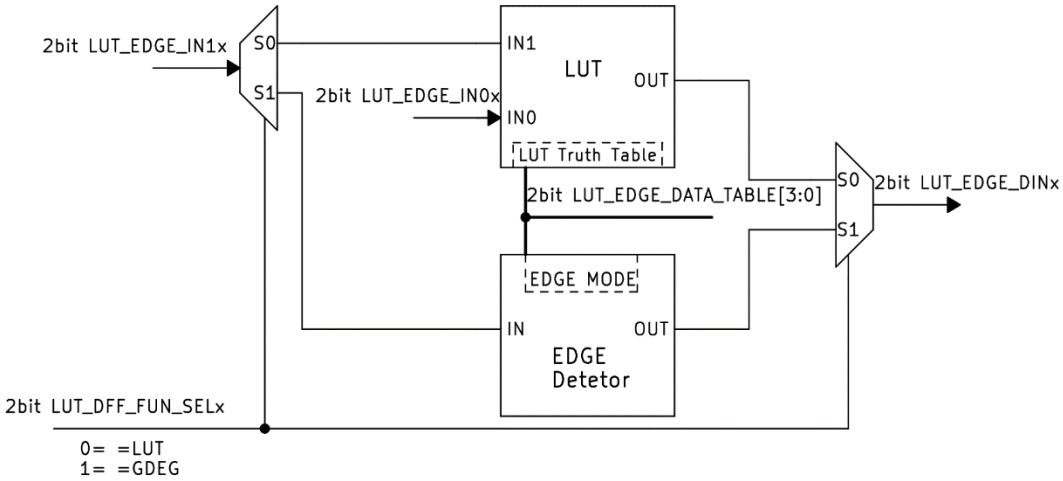


Figure 9：2-bit LUT/Edge Detector

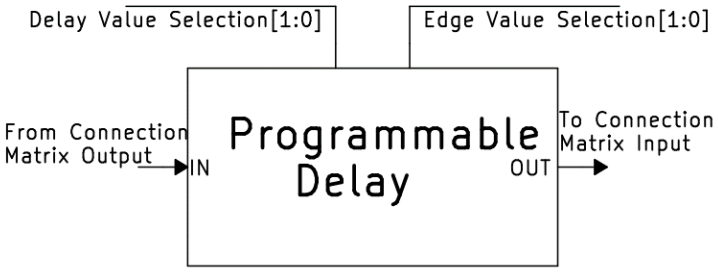


Figure 10：Programmable Delay

6.4 3-bit LUT/Pipe Delay

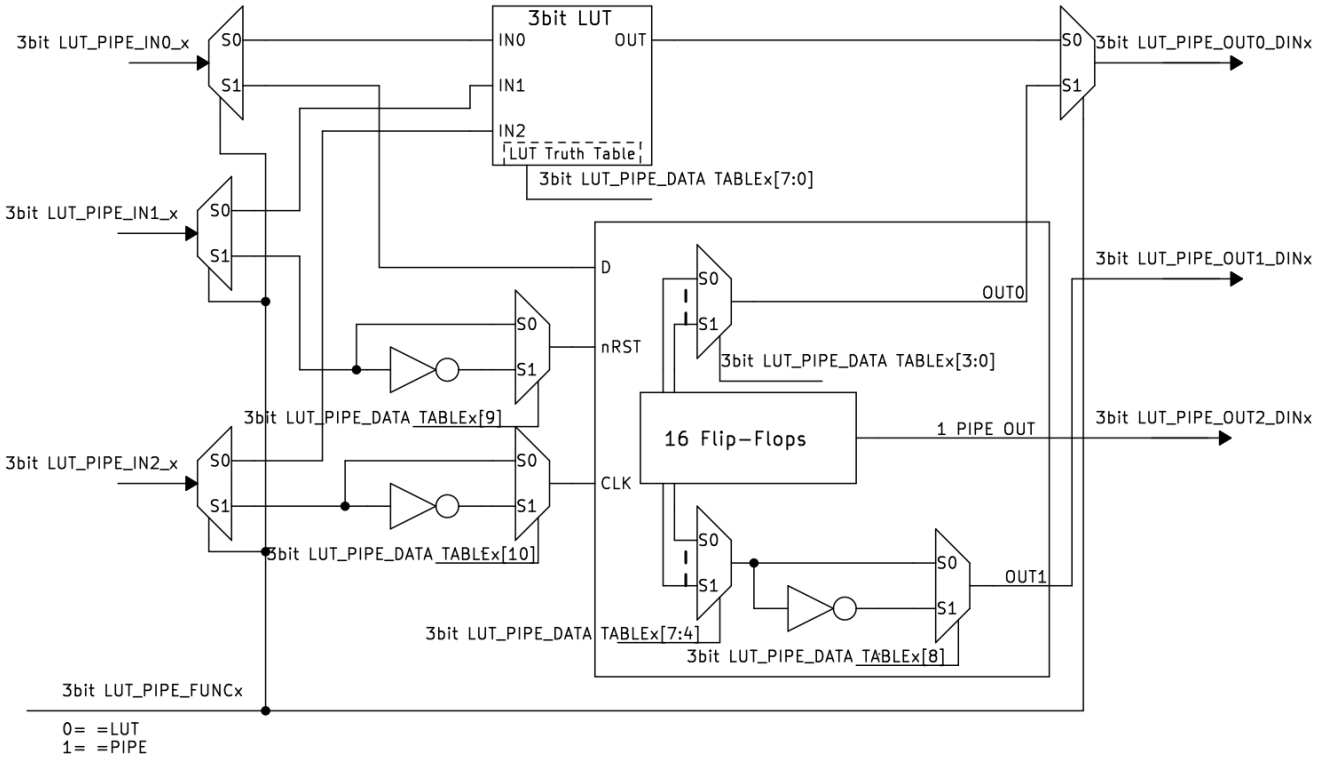


Figure 11：3-bit LUT/Pipe Delay

6.5 4-bit LUT/DFF with nRST/nSET

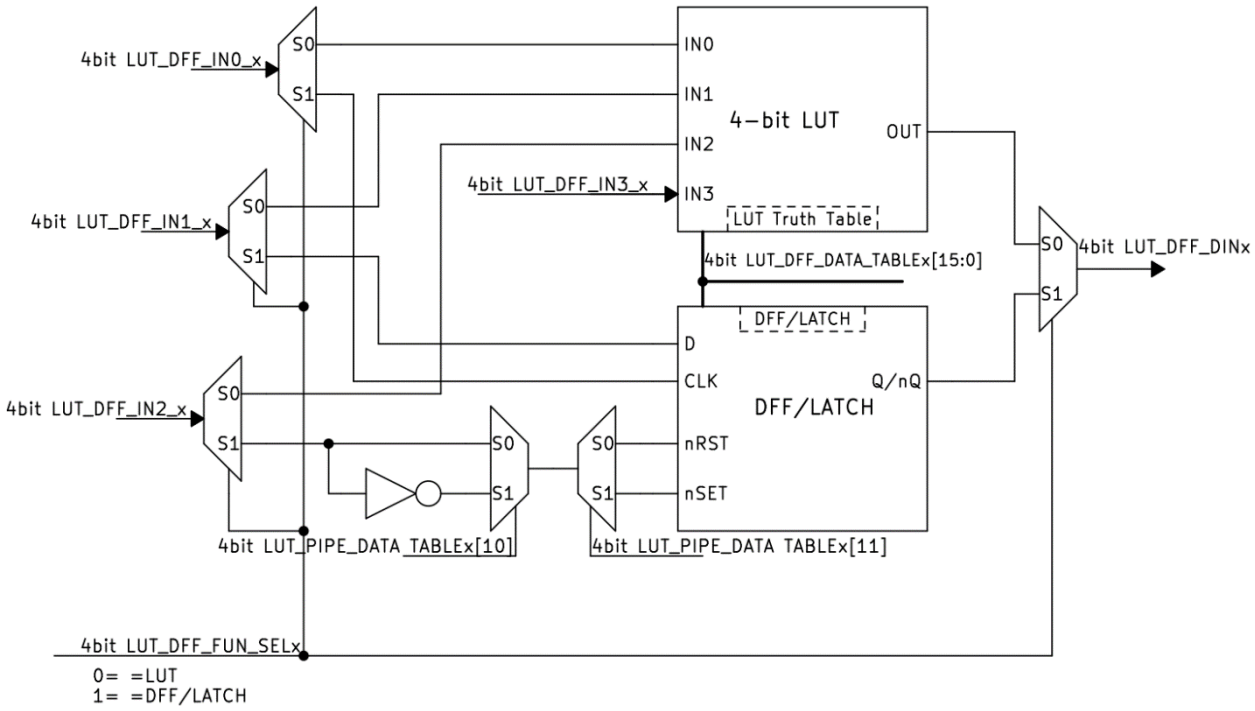


Figure 12：4-bit LUT/DFF

7. Multi-Function Block（MFB）

LS98003 has eight Multi-Function Blocks that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes s such as One Shot, Frequency Detect, Edge Detect, and others. Also, the block is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF.

See the list below for the functions that can be implemented in these blocks:

- Seven Selectable 3-bit LUT/DFF + 8-bit Counter/Delay
- One Selectable 4-bit LUT/DFF + 16-bit Counter/Delay

7.1 3-bit LUT/DFF or 8-bit Counter/Delay Block Diagrams

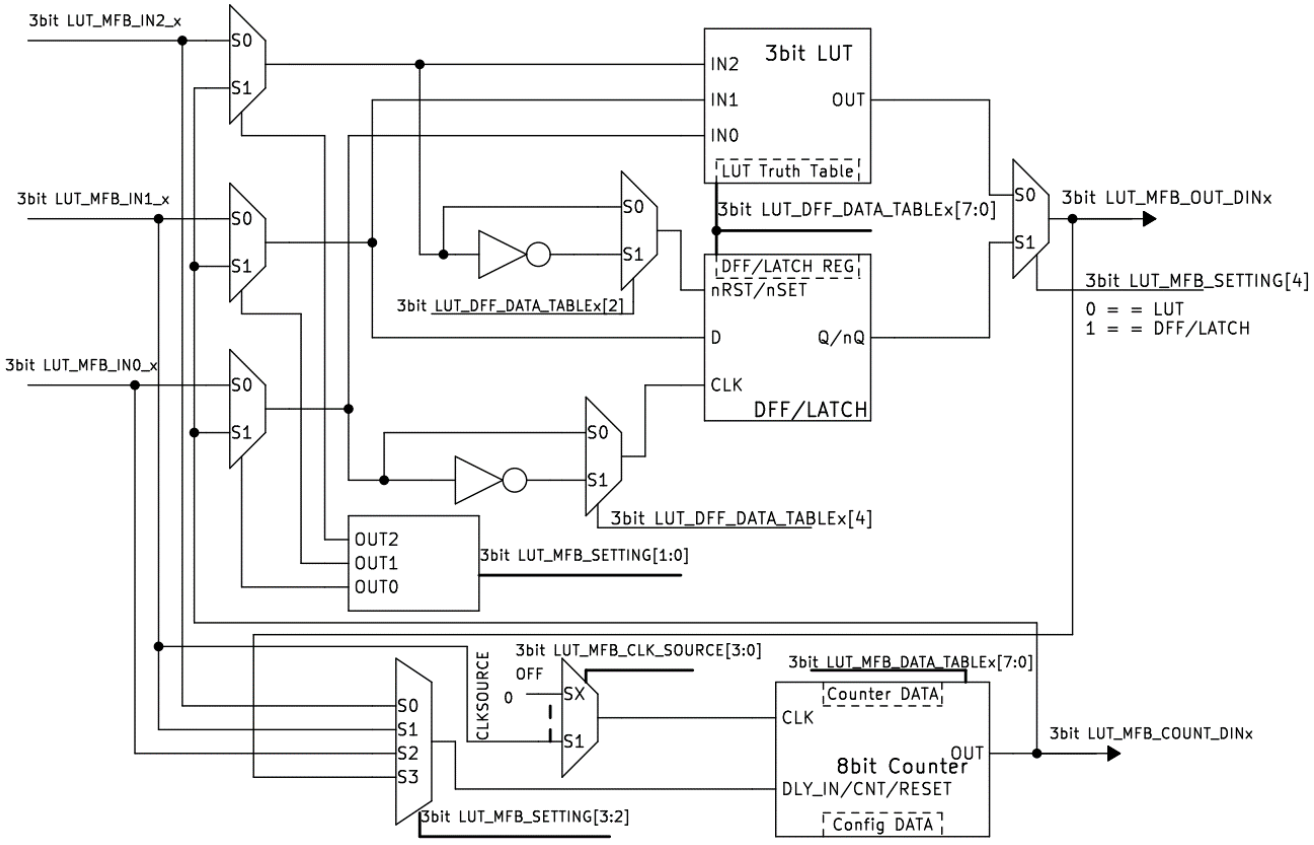


Figure 13：3-bit LUT or 8-bit Counter/Delay

7.2 4-bit LUT/DFF or 16-bit Counter/Delay Block Diagrams

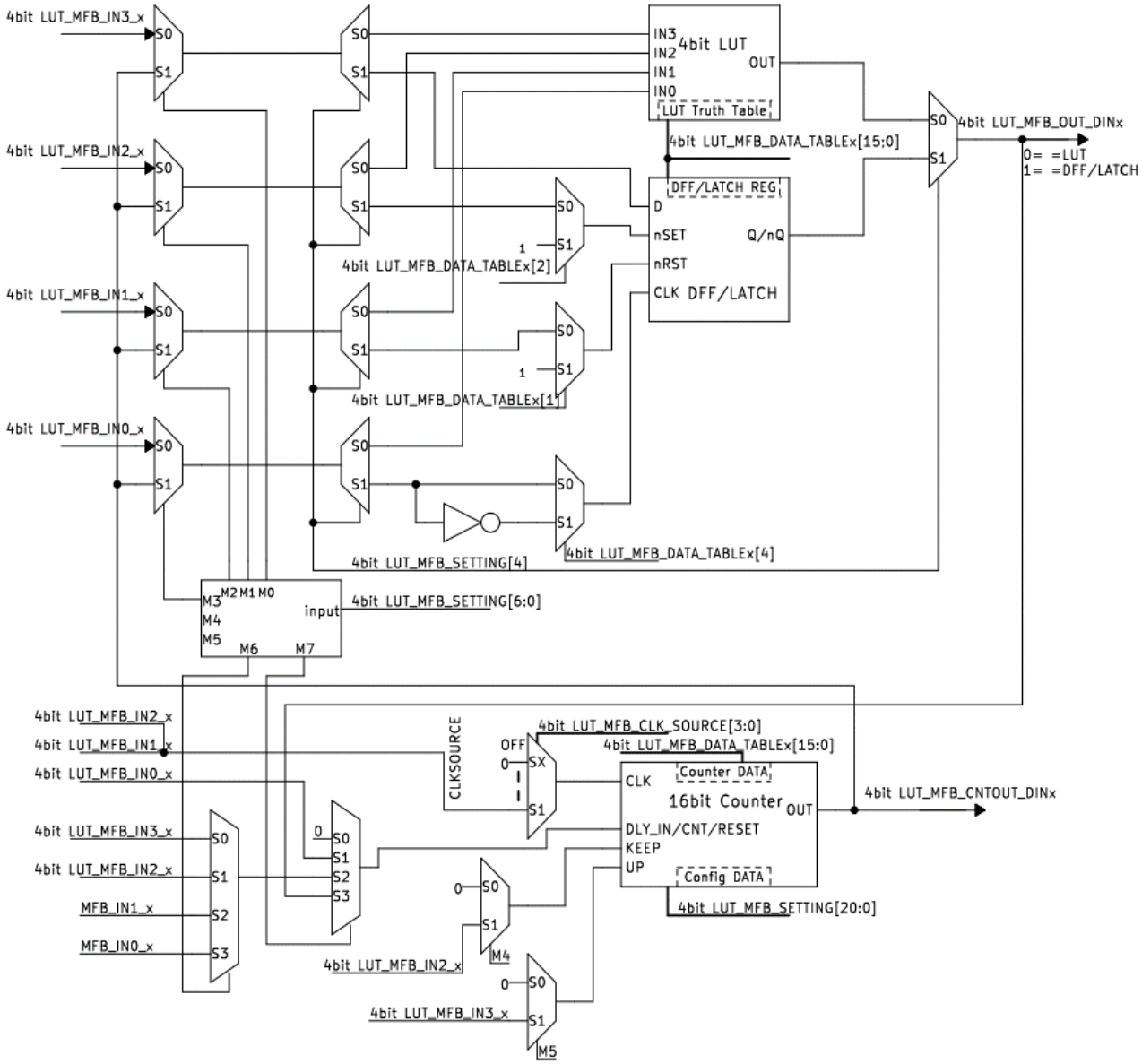


Figure 14：4-bit LUT or 16-bit Counter/Delay

8. I²C Communication Interface

The LS98003 provides an I²C communication interface that allows the I²C master to read or write internal registers, thereby remotely reconfiguring internal resources and their connection relationships.

8.1 I²C Read

8.1.1 Current Address Read Command

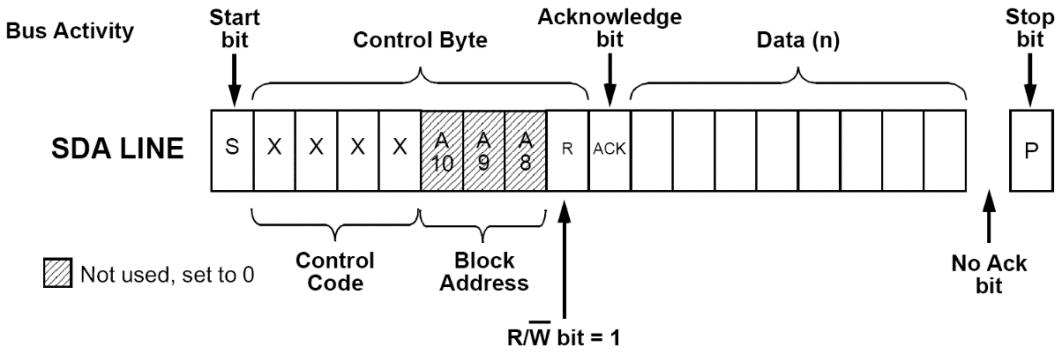


Figure 15：Current Address Read Command

8.1.2 Random Read Command

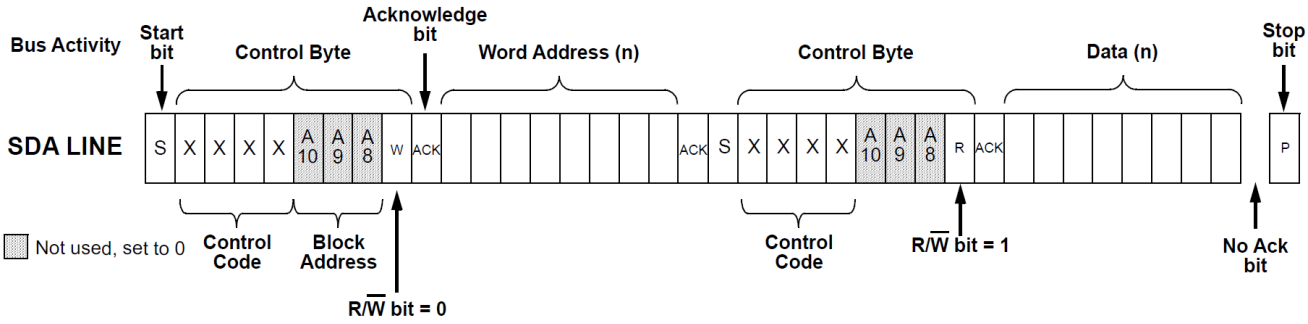


Figure 16：Random Read Command

8.1.3 Sequential Read Command

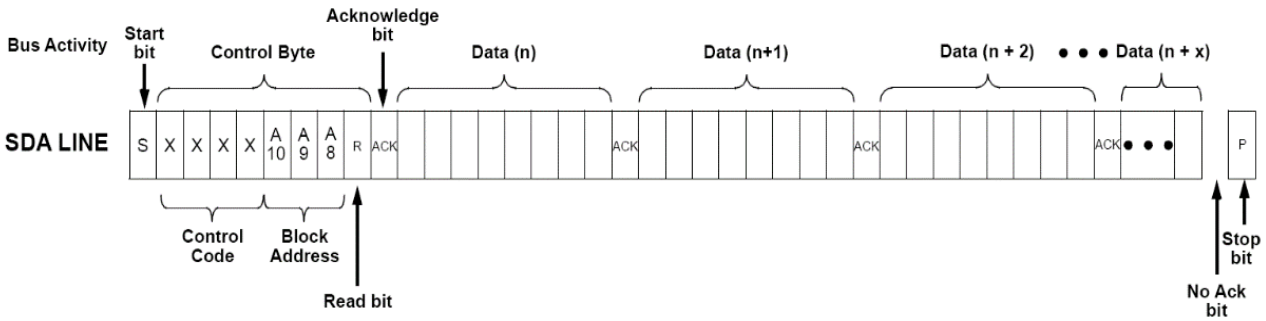


Figure 17：Sequential Read Command

8.2 I²C Write

8.2.1 Byte Write Command

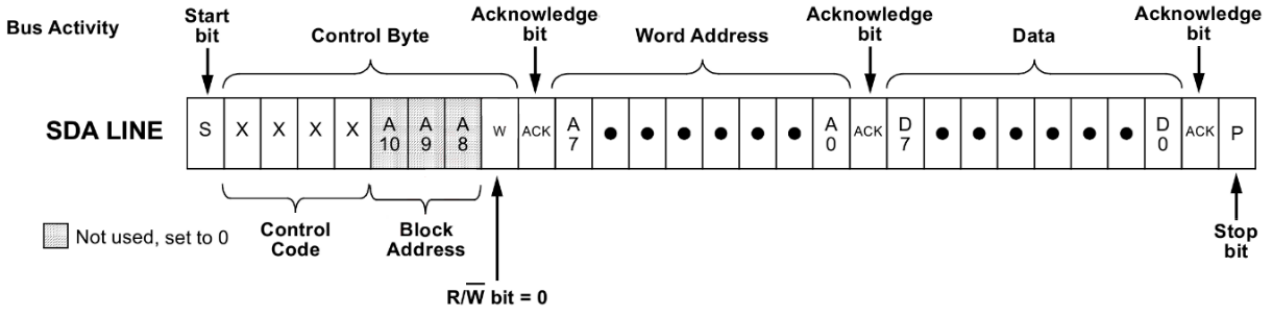


Figure 18：Byte Write Command

8.2.2 Sequential Write Command

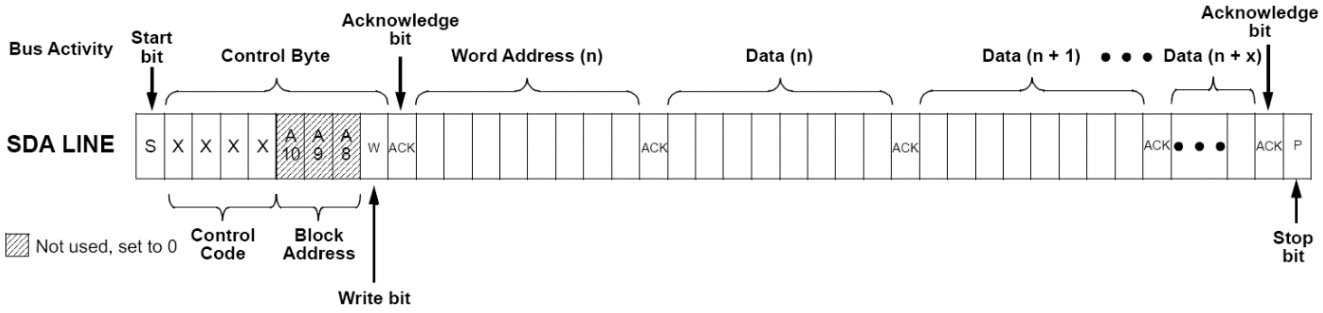


Figure 19：Sequential Write Command

8.3 I²C Timing Diagram

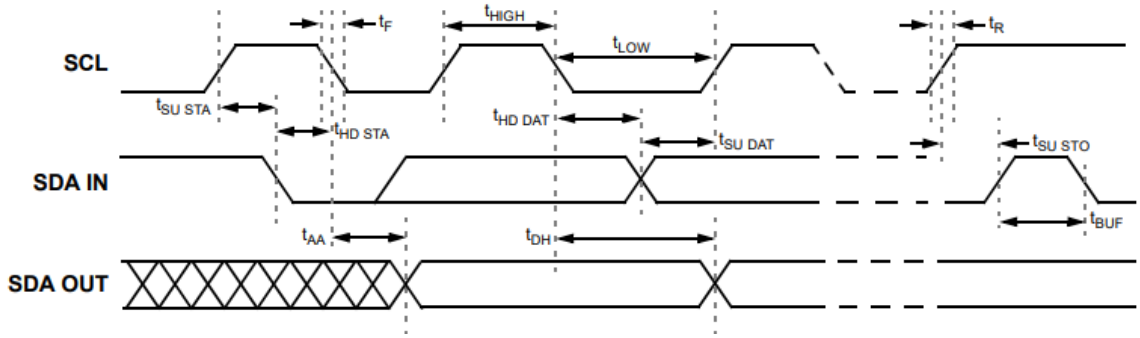


Figure 20：I²C Timing Diagram

8.4 I²C Software Reset Function

If the I²C serial communication is established, the device can be reset to its initial power-on conditions, including the configuration of all Macrocells and all connections provided by the connection matrix. It is achieved by setting register [909] and resetting I²C to "1", which causes the device to enable again the POR sequence, including reloading all register data from NVM. During the POR sequence, the output of the device will be in tristate, and after the reset is completed, the value of the content register [909] will be automatically set to "0".

9. Clock Schem

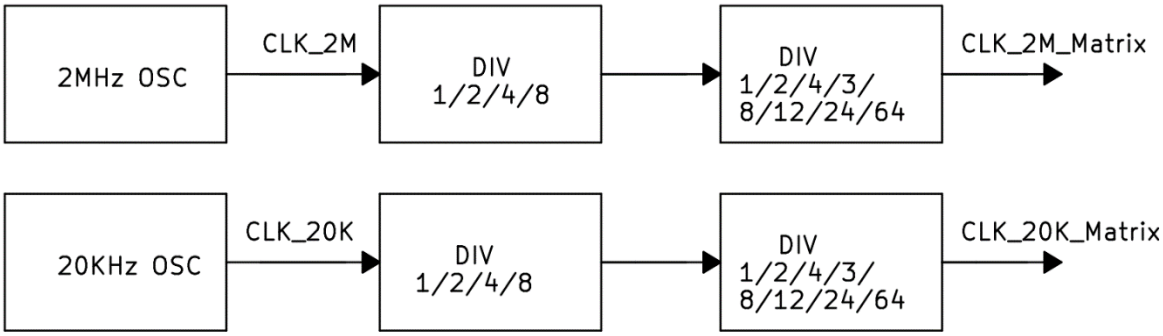


Figure 21：Clock Schem

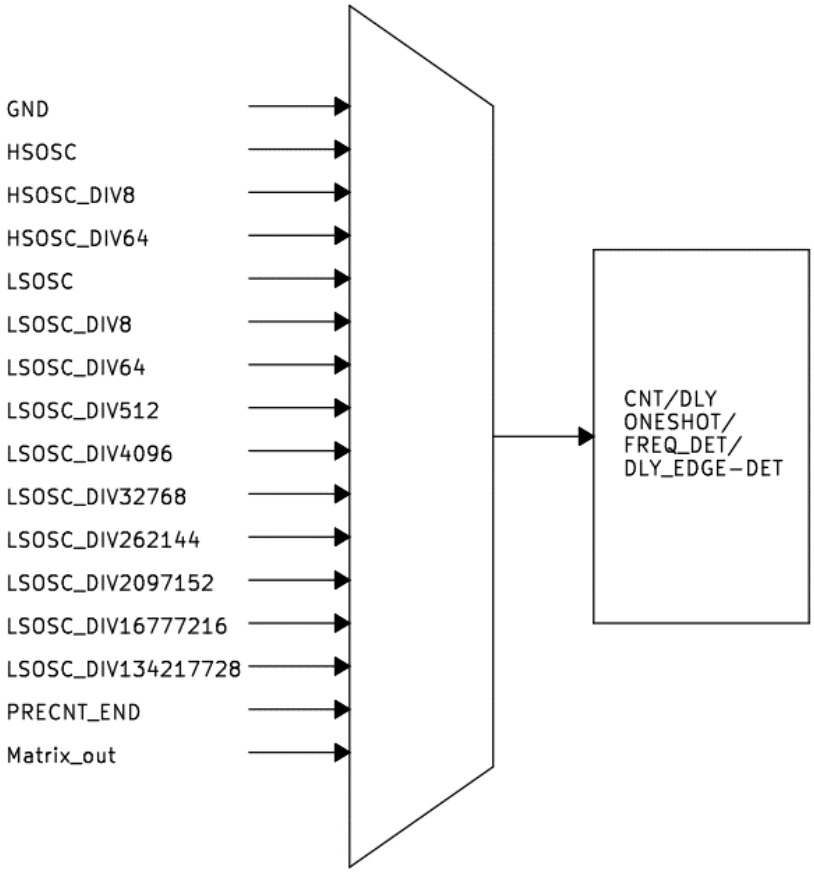


Figure 22：Clock allocation diagram

10. External Clock

LS98003 supports multiple ways to use external high-precision clocks as internal operation reference sources.

10.1 Matrix Source for 20KHz/2MHz Clock

2MHz Clock comes from PIN6, 20KHz Clock comes from PIN2.

11. Code protection function

LS98003 provides the customer with a code protection function, when the protection bit [911] is program into "1", then all chip function related code can be locked, can not be read out, effectively protect the customer's design information.

12. POR

12.1 Power Down

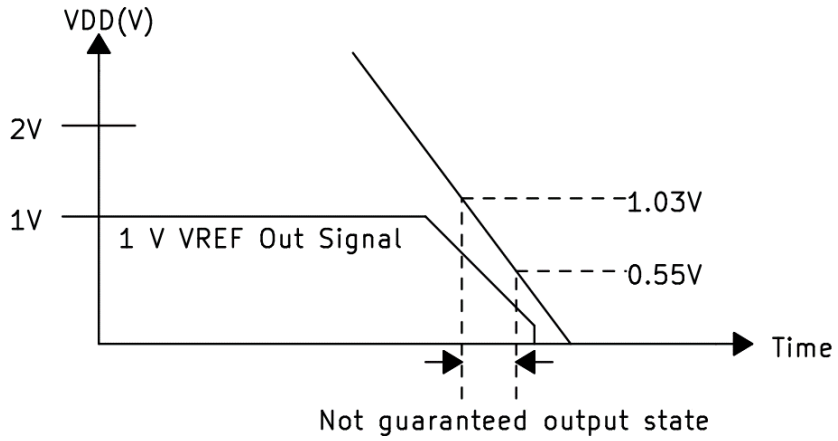


Figure 23：Power Down

During the power down process, when the VDD drops below the Power off Threshold, all macrocells in the LS98003 will be close down. Please take notice that during the slow frequency down period, the output may switch states during this period.

12.2 POR Sequence

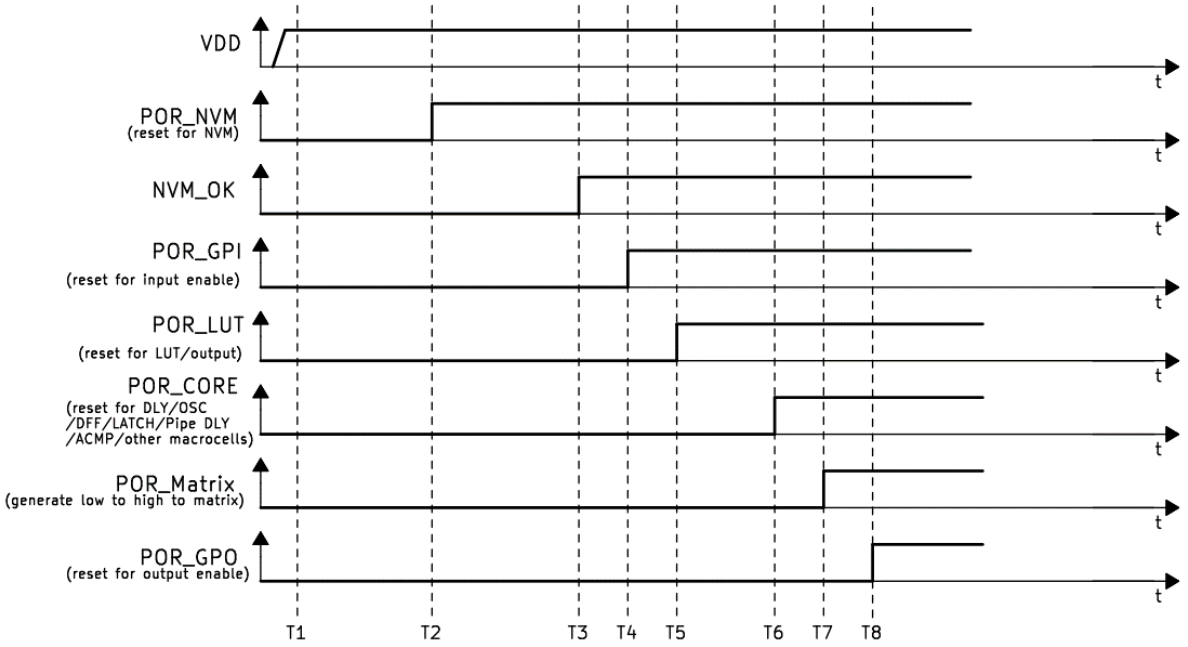


Figure 24：POR Sequence

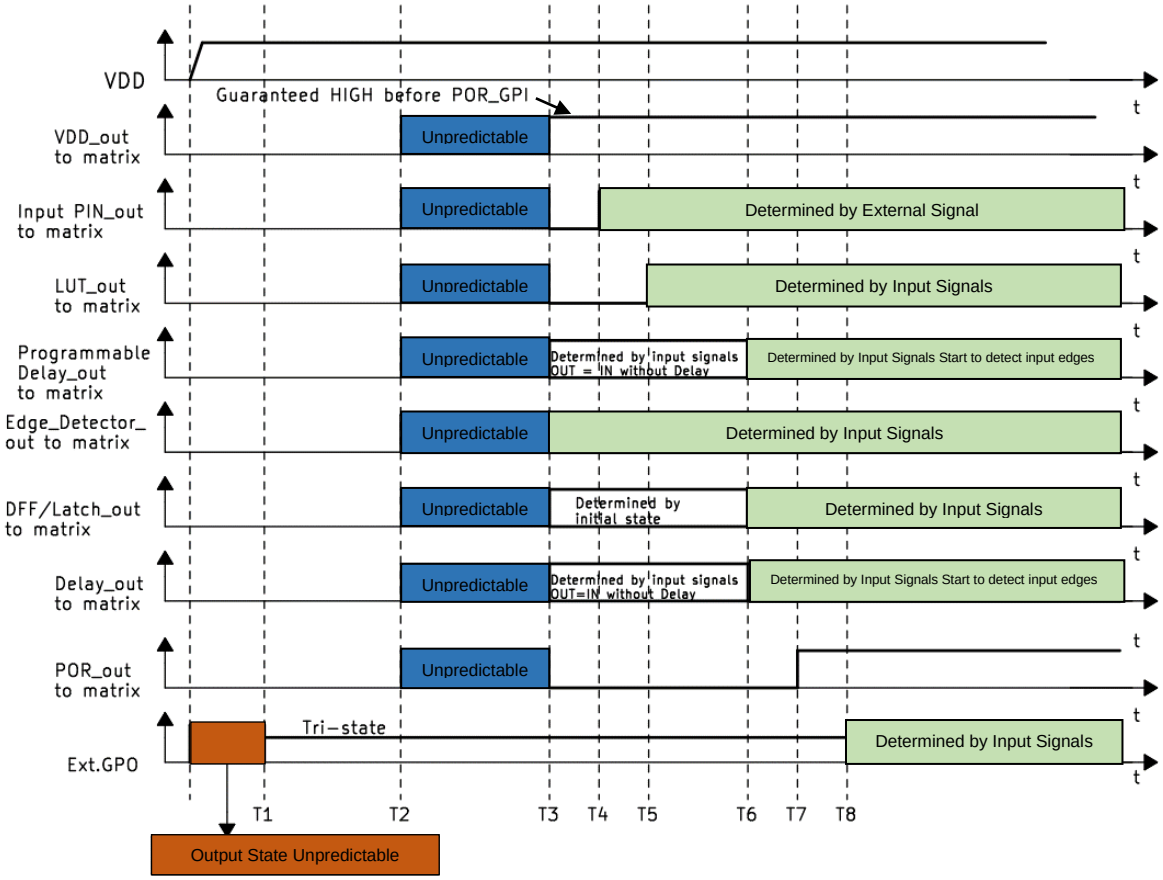


Figure 25：Internal Macrocell States during POR sequence

Note: T1-T8 in Figure 24 and Figure 25 correspond one-to-one.

13. Virtual Memory

13.1 Virtual Memory Input

I²C can write register bit [975:968] into the input of the main matrix<39:32>.

13.2 Virtual Memory Output

I²C can read the output of internal nodes through register [999:992], and the following is the relevant configuration information：

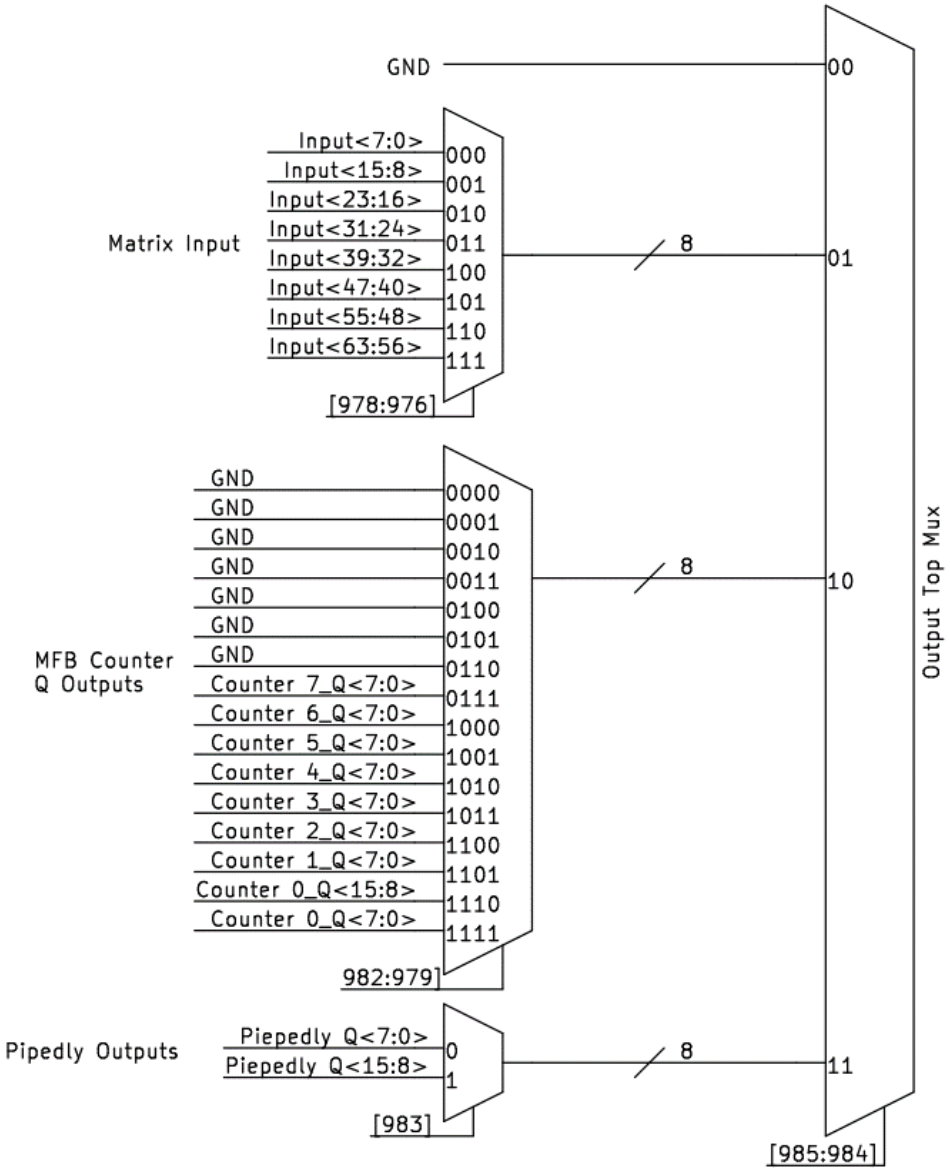
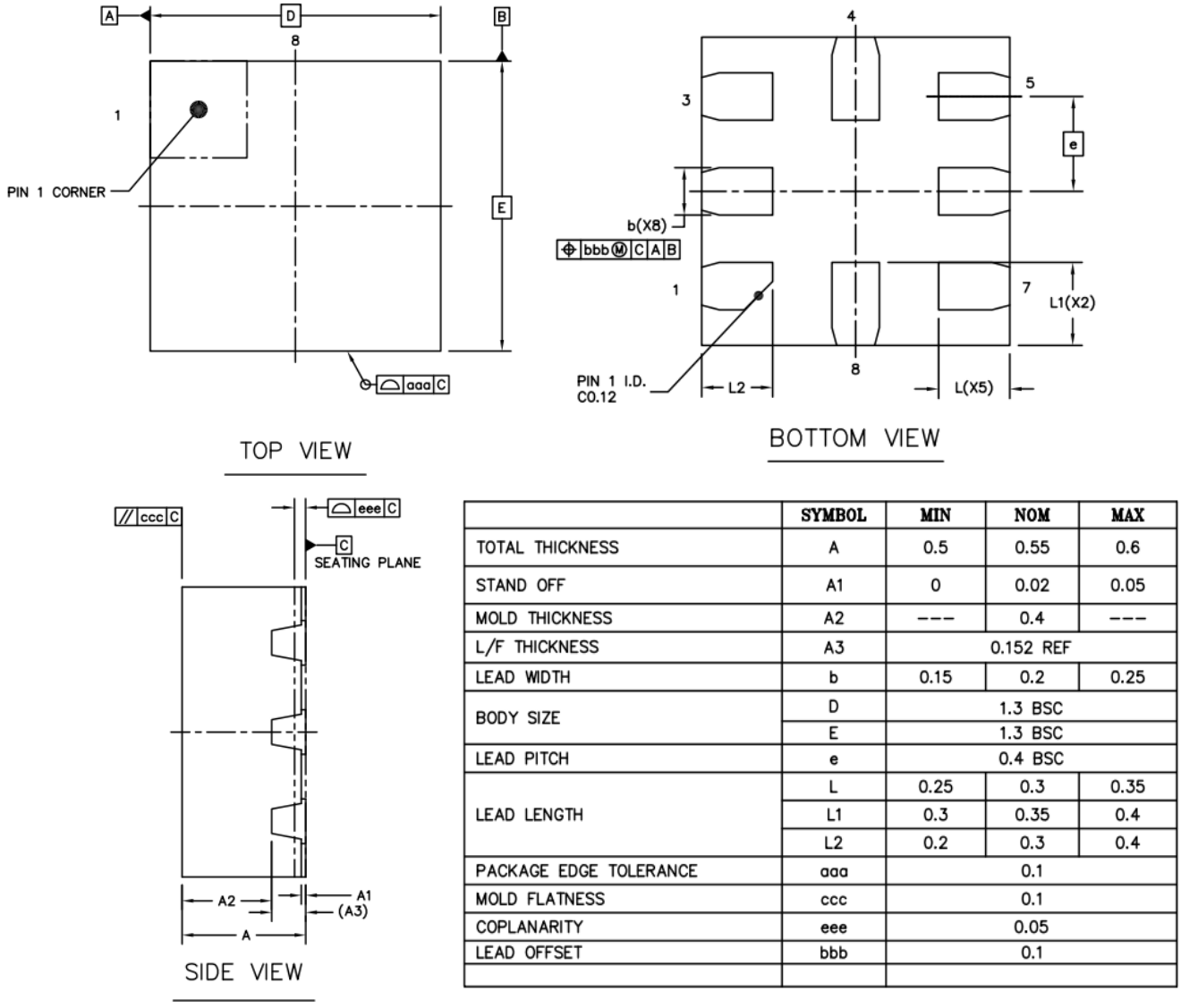


Figure 26：Virtual Memory Out

14. Package Information

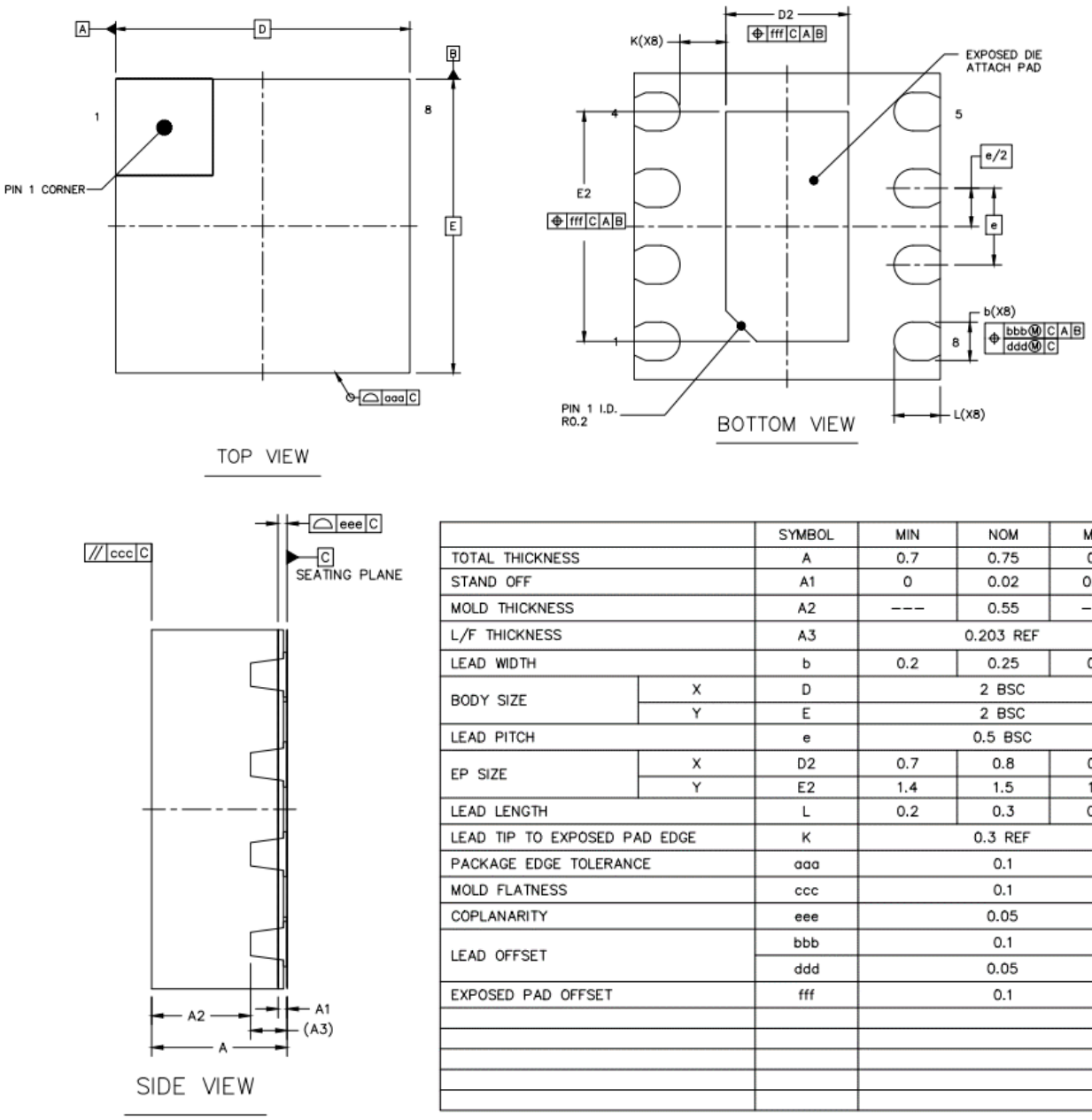
14.1 TQFN-8L:1.3×1.3×0.55mm 0.4mm pitch(LS98003-A)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.5	0.55	0.6
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.4	---
L/F THICKNESS	A3		0.152 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE	D		1.3 BSC	
	E		1.3 BSC	
LEAD PITCH	e		0.4 BSC	
LEAD LENGTH	L	0.25	0.3	0.35
	L1	0.3	0.35	0.4
	L2	0.2	0.3	0.4
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.05	
LEAD OFFSET	bbb		0.1	

Figure 27：Package Outline Diagram

14.2 DFN-8L:2×2×0.75mm 0.5mm pitch(LS98003-D)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		2 BSC	
	Y	E		2 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	0.7	0.8	0.9
	Y	E2	1.4	1.5	1.6
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

Figure 28：Package Outline Diagram

15. Ordering Information

15.1 Tape and Reel Information(LS98003-A)

Table 11：Package Type

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
TQFN-8L 1.3×1.3mm	8	1.3×1.3×0.55	3000	3000	178/60	30	120	140	560	8	4

15.2 Carrier Tape Drawing and Dimensions(LS98003-A)

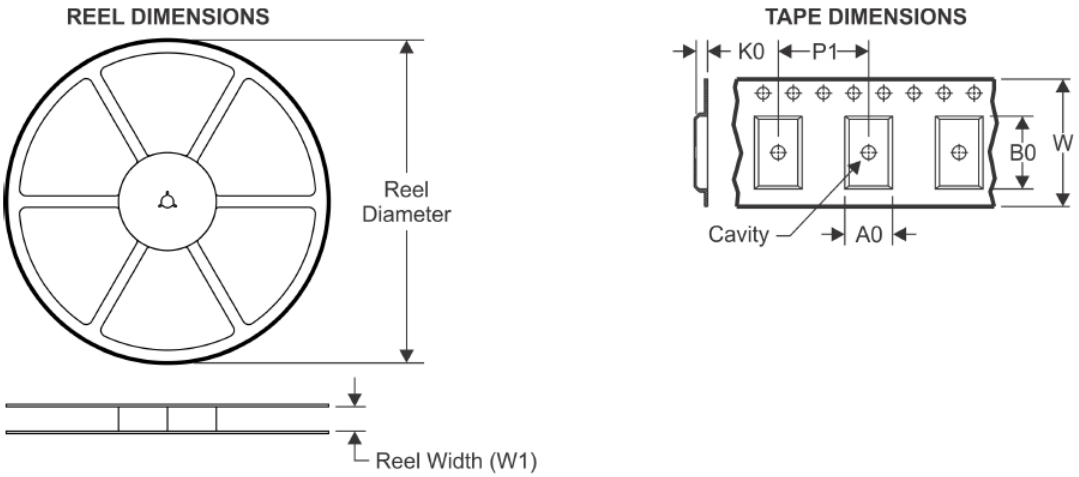


Figure 29：Carrier Tape Drawing and Dimensions

Table 12：Carrier Tape Drawing and Dimensions（LS98003-A）

A0	Dimension designed to accommodate the component width	1.6mm
B0	Dimension designed to accommodate the component length	1.6mm
K0	Dimension designed to accommodate the component thickness	0.8mm
W	Overall width of the carrier tape	8.0mm
W1	Reel Width	9.5mm
P0	Pitch between Index Hole Pitch	4.0mm
P1	Pitch between successive cavity centers	4.0mm

15.3 Tape and Reel Information(LS98003-D)

Table 13：Package Type

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
DFN-8L 2.0×2.0mm	8	2.0×2.0×0.75	3000	3000	178/60	30	120	140	560	8	4

15.4 Carrier Tape Drawing and Dimensions(LS98003-D)

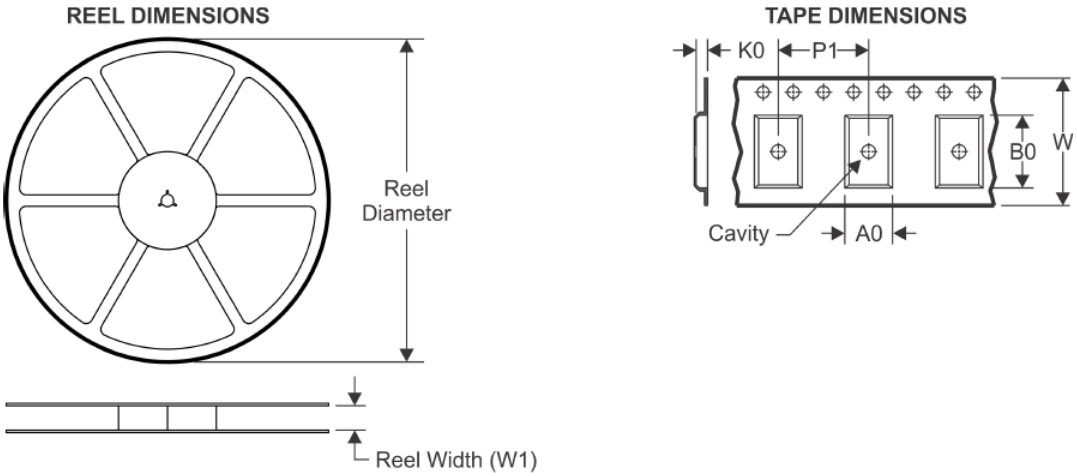


Figure 30：Carrier Tape Drawing and Dimensions

Table 14：Carrier Tape Drawing and Dimensions（LS98003-D）

A0	Dimension designed to accommodate the component width	2.3mm
B0	Dimension designed to accommodate the component length	2.3mm
K0	Dimension designed to accommodate the component thickness	1.1mm
W	Overall width of the carrier tape	8.0mm
W1	Reel Width	9.5mm
P0	Pitch between Index Hole Pitch	4.0mm
P1	Pitch between successive cavity centers	4.0mm

16. Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020

16.1 Recommended Land Pattern(LS98003-A)

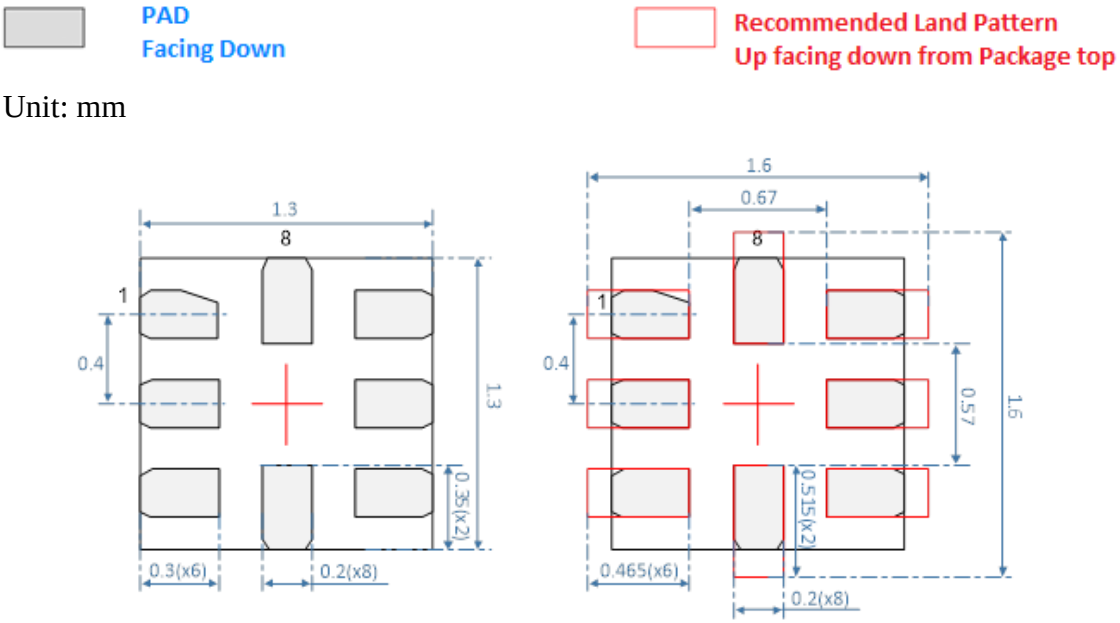


Figure 31：Recommended Land Pattern (LS98003-A)

16.2 Recommended Land Pattern(LS98003-D)

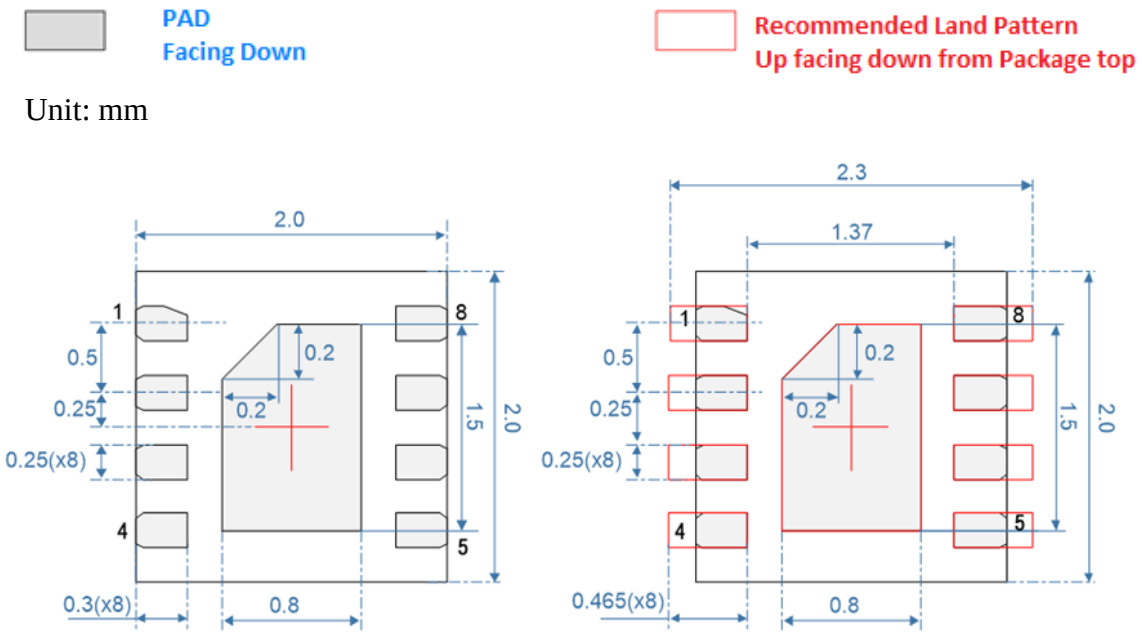


Figure 32：Recommended Land Pattern（LS98003-D）

17. Revision History

Table 15：Revision History

Version	Revision Contents	Revised By	Date
R01	Initial version		2023-10-10
R02	According to the test data, the Max value of IO PIN module V_{IL} parameter in Table 7 to Table 8 under 'Low-Level Logic Input' conditions is 0.63 updated to 0.75 and 0.71 updated to 0.85 respectively. (P11 and P12).		2024-01-06
R03	1. Color identification in Figure 25. (P25) 2. There is an error in the PIN identification in Figure 32. The PIN identification for "5 and 6" has been changed to "4 and 5" respectively. (P31) 3. According to the software calculation, the Max values of the IO PIN module V_{IL} parameter 'LowLevel Logic Input' in Tables 7 to 8 are updated from '0.75 to 0.77', and from '0.85 to 0.86' respectively (P11, P12)		2024-03-19